

FINOLEX ACDAEMY OF MANAGEMENT & TECHNOLOGY, RATNAGIRI.

DEPT. OF ELECTRONICS ENGG.

Name of the laboratory: - VLSI LAB.

LIST OF EXPERIMENTS.

1	Design and implementation of 4 bit adder using VHDL.
2	Design and implementation of 1 bit ALU using VHDL and implementing and verifying the design in XILINX CPLD9572.
3	Design and simulation of NMOS inverter using PSPICE.
4	Design and simulation of CMOS inverter using PSPICE.
5	Design and simulation of two input CMOS NAND gate using PSPICE.
6	Design and simulation of two input CMOS NOR gate using PSPICE.
7	Layout design of CMOS inverter.
8	Layout design of two input CMOS NOR gate.
9	Layout design of two input CMOS NAND gate.
10	Four bit parallel adder using structural level abstraction.
11	Four bit adder using data flow modeling.
12	Switch Level XOR and OR gates.
13	One bit adder using switch level modeling.
14	Sequence detector.
15	One bit mirror adder using SPICE AD.